a conductive plug formed of a single conductive material positioned within an insulator layer and provided over said active region, said conductive plug being electrically connected with said active region;

an etch-stop layer deposited on said insulator and around said conductive plug;

an intermediate non-conductive layer provided over said etch stop layer and having at least a first and a second etched via over said plug, wherein said second etched via is above and has a greater diameter than said first etched via; and

a first conductive layer deposited in and in contact with said first and second vias, said first conductive layer including a portion in contact with said conductive plug, and a second conductive layer deposited over and in contact with said first conductive layer.

C1 cont

C2

E1

15. (Amended) The semiconductor memory device of claim 11, wherein said first conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

16. (Amended) The semiconductor memory device of claim 11, wherein said second conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, titanium, titanium nitride and tungsten.

C3 Sub D3

25. (Twice Amended) A processor-based system comprising:

a processing unit;

a semiconductor circuit coupled to said processing unit, said semiconductor circuit comprising:

a conductive plug formed of a single conductive material positioned within an insulator and provided on a connection region;

an etch-stop layer deposited on said insulator, said etch-stop layer being at the same level as a top portion of said conductive plug;

an intermediate non-conductive layer provided over said etch-stop layer and having at least a first and a second etched via over said conductive plug, wherein said second etched via is above and has a greater diameter than said first etched via; and

a conductive connector electrically coupled to said connection region, said conductive connector comprising a first conductive layer deposited in and in contact with said first and second etched vias, said first conductive layer including a portion in contact with said conductive plug, and a second conductive layer deposited over and in contact with said first conductive layer.

C4 E1

27. (Amended) The processor-based system of claim 25, wherein said connection region comprises a doped region within said substrate.

28. (Amended) The processor-based system of claim 25, wherein said intermediate layer comprises doped silicate glass.

30. (Amended) The processor-based system of claim 25, wherein said first conductive layer comprises at least one layer of one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

31. (Amended) The processor-based system of claim 25, wherein said second conductive layer comprises at least one layer of one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

32. (Amended) The processor-based system of claim 25, further comprising a substrate, and wherein said connection region is located in said substrate, and wherein said conductive plug is located over said connection region.